Evaluation Board for Filterless Class-D Audio Amplifier

EVAL-SSM2315

FEATURES

Single-ended and differential input capability
Multiple input interface connection options (jack or header)
Optimized EMI suppression filter assembled on board
PCB footprint for dc power supply jack (accepts 2.5 V to 5.5 V)

GENERAL DESCRIPTION

The SSM2315 is a fully integrated, single-chip, mono Class-D audio amplifier. It is designed to maximize performance for mobile phone applications. The application circuit requires a minimum of external components and operates from a single 2.5 V to 5.5 V supply. It is capable of delivering 3 W of continuous output power with less than 1% THD + N driving a 3 Ω load from a single 5.0 V supply.

The SSM2315 comes with a differential mode input port and a high efficiency, full H-bridge at the output that enables direct coupling of the audio power signal to the loudspeaker. The differential mode input stage allows for canceling of common-mode noise.

The part also features a high efficiency, low noise output modulation scheme that requires no external LC output filters when attached to an inductive load. The modulation provides high efficiency even at low output power. Filterless operation also helps to decrease distortion due to the nonline-arities of output LC filters.

This data sheet describes how to configure and use the SSM2315 evaluation board to test the SSM2315. It is recommended that this data sheet be read in conjunction with the SSM2315 data sheet, which provides more detailed information about the specifications, internal block diagrams, and application guidance for the amplifier IC.

EVALUATION BOARD DESCRIPTION

The SSM2315 evaluation board carries a complete application circuit for driving a loudspeaker. Figure 1 shows the top view of the evaluation board, and Figure 2 shows the bottom view.

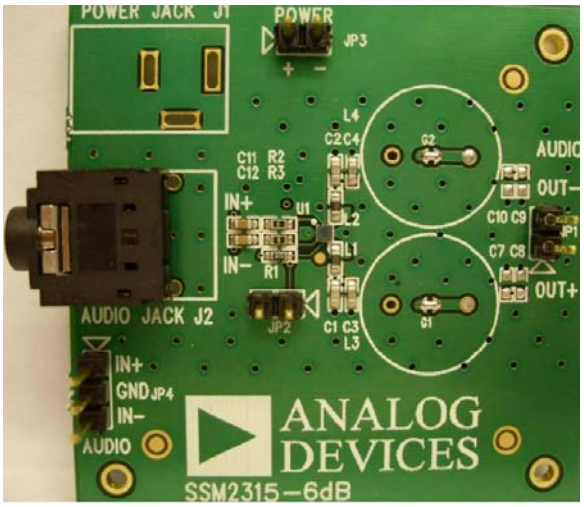

Figure 1. SSM2315 Evaluation Board Top View

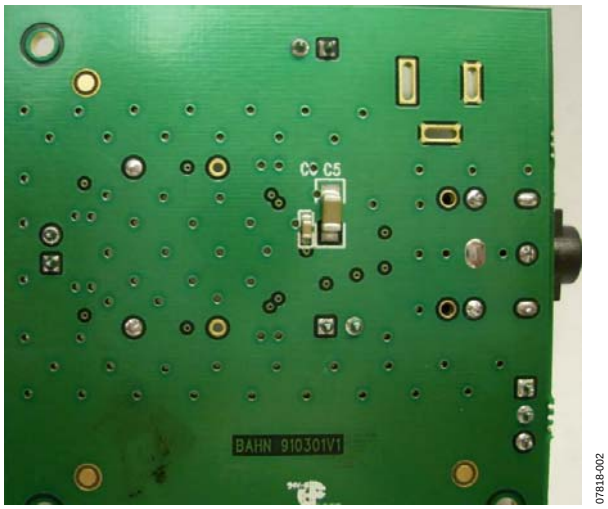

Figure 2. SSM2315 Evaluation Board Bottom View

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

Features 1
General Description 1
Evaluation Board Description 1
Revision History 2
Evaluation Board Hardware 3
Input Configuration 3
Output Configuration 3
Power Supply Configuration 3
Component Selection 3
PCB Layout Guidelines 4
Getting Started 5
What to Test 5
Evaluation Board Schematic and Artwork 6
Ordering Information 9
Bill of Materials 9
Ordering Guide 9
ESD Caution 9

REVISION HISTORY

5/09—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

INPUT CONFIGURATION

On the left side of the board below the power jack, there is a standard 3.5 mm audio stereo jack connector, J2 (see Figure 1). Below J2 is a 3-pin header (JP4). These headers are used to feed the audio signal into the board.

If the input audio signal is differential (IN+ and IN−), use either J2 or JP4. In this case, all three pins of JP4 are used for IN+, IN−, and the ground.

For a single-ended audio input, using JP4 as the input connector is recommended. In this case, only two pins of JP4 are used: one pin is for the ground and the other is for either IN+ or IN−. If IN+ is used, place a jumper between Pin 2 and Pin 3 of JP4, shorting IN− to ground. If IN− is used, place the jumper between Pin 1 and Pin 2 of JP4, connecting IN+ to ground.

The two-pin header, JP2, is used to turn the SSM2315 amplifier on and off. Putting a jumper on JP2 shuts down the SSM2315 so that only a minimum current (about 20 nA) is drawn from the power supply. Removing the jumper puts the SSM2315 in normal operating mode.

OUTPUT CONFIGURATION

The output connector, JP1, is located on the right side of the board. JP1 drives a loudspeaker whose impedance should be no less than 3 Ω.

The SSM2315 does not require any external LC output filters because it has a low noise modulation scheme. However, if the speaker length is >10 cm, it is recommended that a ferrite bead (L1 and L2) be placed near each output pin of the SSM2315 to reduce electromagnetic interference (EMI), as shown in the schematic in Figure 4.

On the board, there are two inductors, L3 and L4, that are not loaded and are not required for normal operation (they are shorted by the solder gaps, G1 and G2). Some users may want to add these inductors to evaluate certain applications with tighter EMI vs. audio performance constraints. If L3 and L4 are loaded, the solder on G1 and G2 must be removed with a soldering iron.

As an aid, a properly tuned ferrite bead based EMI filter is assembled at the output terminals of the device. For optimal performance, as specified in the SSM2315 data sheet (in particular, for THD and SNR), remove the entire EMI filter, short across the ferrite bead terminals, and open the capacitor terminals.

POWER SUPPLY CONFIGURATION

The schematic for the evaluation board is shown in Figure 4. There is a PCB footprint to populate a standard power jack (J1), which accepts a 2.5 V to 5.5 V dc power supply (see the upper left corner of Figure 1). For most laboratory measurement setups, use the 2-pin header (JP3) to power the board. In either case, care must be taken to connect the dc power with correct polarity and voltage. The J1 jack is not populated during PCB assembly.

Polarity and Voltage

The wrong power supply polarity or overvoltage may permanently damage the board. The maximum peak current is approximately 0.33 A when driving an 8 Ω load and when the input voltage is 5 V.

COMPONENT SELECTION

Selecting the proper components is the key to achieving the performance required at the cost budgeted.

Input Coupling Capacitor Selection—C11 and C12

The input capacitors, C11 and C12, should be large enough to couple the low frequency signal components in the incoming signal but small enough to filter out unnecessary low frequency signals. For music signals, the cutoff frequency chosen is often between 20 Hz and 30 Hz. The value of the input capacitor is calculated by

$$C = 1/(2\pi Rf_c)$$

where:
R = 80 kΩ + R_{EXT} (the external resistor used to fine-tune the desired gain; on the schematic (see Figure 4), this is the 0 Ω resistor at the input pins).
f_c is the cutoff frequency.

Output Ferrite Beads—L1 and L2

The L1 and L2 output beads are necessary components for filtering out the EMI caused at the switching output nodes when the length of the speaker wire is greater than 10 cm. The penalty for using ferrite beads for EMI filtering is slightly worse noise and distortion performance at the system level due to the nonlinearity of the beads.

Ensure that these beads have enough current conducting capability while providing sufficient EMI attenuation. The current rating needed for an 8 Ω load is approximately 420 mA, and impedance at 100 MHz must be ≥120 Ω. In addition, the lower the dc resistance (DCR) of these beads, the better for minimizing their power consumption.

Table 1 describes the recommended beads.

Table 1. Recommended Output Beads (L1 and L2)

Part No.	Manufacturer	Z (Ω)	I_{MAX} (mA)	DCR (Ω)	Size (mm)
BLM18PG121SN1D	Murata	120	2000	0.05	1.6 × 0.8 × 0.8
MPZ1608S101A	TDK	100	3000	0.03	1.6 × 0.8 × 0.8
MPZ1608S221A	TDK	220	2000	0.05	1.6 × 0.8 × 0.8
BLM18EG221SN1D	Murata	220	2000	0.05	1.6 × 0.8 × 0.8

Table 2. Recommended Output Inductors (L3 and L4)

Part No.	Manufacturer	L (µH)	I_{MAX} (mA)	DCR (Ω)	Size (mm)
LQM31PNR47M00	Murata	0.47	1400	0.07	3.2 × 1.6 × 0.85
LQM31PN1R0M00	Murata	1.0	1200	0.12	3.2 × 1.6 × 0.85
LQM21PNR47MC0	Murata	0.47	1100	0.12	2.0 × 1.25 × 0.5
LQM21PN1R0MC0	Murata	1.0	800	0.19	2.0 × 1.25 × 0.5
LQH32CN2R2M53	Murata	2.2	790	0.1	3.2 × 2.5 × 1.55

Output Shunting Capacitors

There are two groups of output shunting capacitors: C1, C2, C3, and C4 work with the L1 and L2 ferrite beads; C7, C8, C9, and C10 work with L3 and L4, if they are used. Use small size (0603 or 0402) multilayer ceramic capacitors that are made of X7R or COG (NPO) materials. Note that the capacitors can be used in pairs: a capacitor with small capacitance (up to 100 pF) plus a capacitor with a larger capacitance (less than 1 nF). This configuration provides thorough EMI reduction for the entire frequency spectrum. For BOM cost reduction and capable performance, a single capacitor of approximately 470 pF can be used.

Output Inductors—L3 and L4

If you prefer using inductors for the purpose of EMI filtering at the output nodes, choose inductance that is < 2.2 µH. The higher the inductance, the lower the EMI is at the output. However, the cost and power consumption by the inductors are higher. Using 0.47 µH to 2.2 µH inductors is recom-mended, and the current rating needs >600 mA (saturation current) for an 8 Ω load. Table 2 shows the recommended inductors. Note that these inductors are not populated on the evaluation board.

PCB LAYOUT GUIDELINES

To keep the EMI under the allowable limit and to ensure that the amplifier chip operates under the temperature limit, PCB layout is critical in application design. Figure 3 shows the preferred layout for the SSM2315 evaluation board.

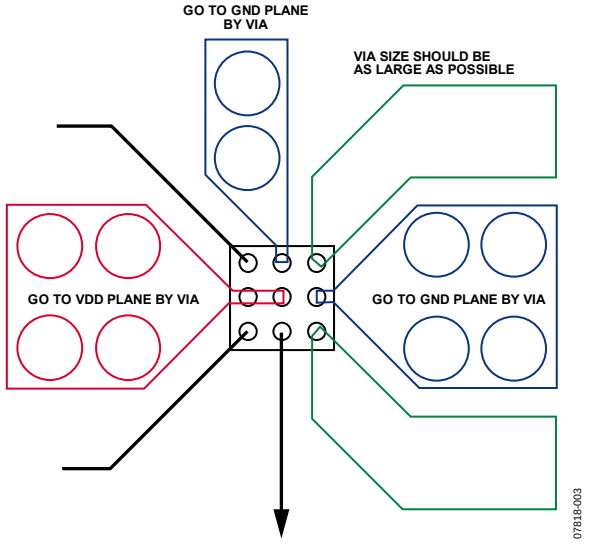

Figure 3. Preferred PCB Layout for the SSM2315 Evaluation Board

Layer Stacks and Grounding

The stack-up for the evaluation board is a 4-layer structure.

- Top layer—component layer with power and output copper land and ground copper pouring.
- Second layer—dedicated ground plane.
- Third layer—dedicated power plane.
- Bottom layer—bottom layer with ground copper pouring.

Component Placement and Clearance

Place all related components except decoupling capacitors on the same side as the SSM2315 and as close as possible to the chip to avoid vias (see Figure 5).

Place decoupling capacitors on the bottom side and close to the GND pin (see Figure 7).

Top Layer Copper Land and Ground Pouring

The output peak current of this amplifier is more than 1 A; therefore, PCB traces should be wide (>2 mm) to handle the high current. For the best performance, use symmetrical copper lands as large as space allows (instead of traces) for the output pins (see Figure 3).

Pour ground copper on the top side and use many vias to connect the top layer ground copper to the dedicated ground plane. The copper pouring on the top layer serves as both the EMI shielding ground plane and the heat sink for the SSM2315.

The SSM2315 works well only if these techniques are implemented in the PCB design to keep EMI and the amplifier temperature low.

GETTING STARTED

To ensure proper operation, carefully follow Step 1 through Step 4.

1. If a jumper is on JP2, remove the jumper to turn on the amplifier.
2. Connect the load to the audio output connector, JP1.
3. Connect the audio input to the board, either in differential mode or single-ended mode, depending on the application.
4. Connect the power supply with the proper polarity and voltage.

WHAT TO TEST

When implementing the SSM2315 evaluation board, test the board for the following items:

- Electromagnetic interference (EMI)—connect wires for the speakers, making sure they are the same length as the wires required for the actual application environment; then complete the EMI test.
- Signal-to-noise ratio (SNR).
- Output noise—use an A-weighted filter to filter the output before reading the measurement meter.
- Maximum output power.
- Distortion.
- Efficiency.

EVALUATION BOARD SCHEMATIC AND ARTWORK

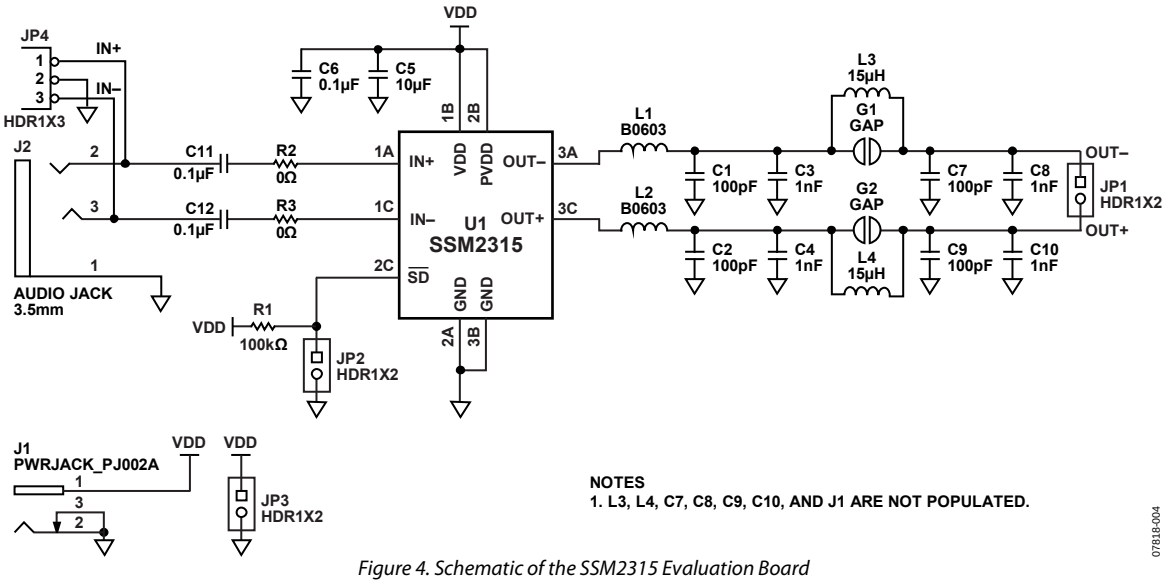

Figure 4. Schematic of the SSM2315 Evaluation Board

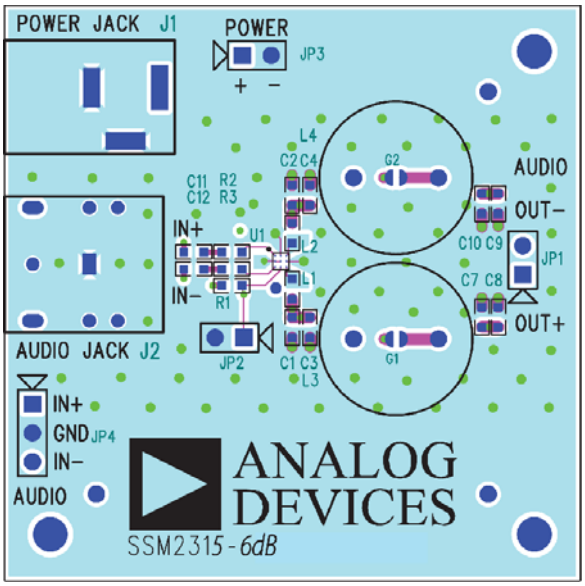

Figure 5. Top Layer with Top Silkscreen

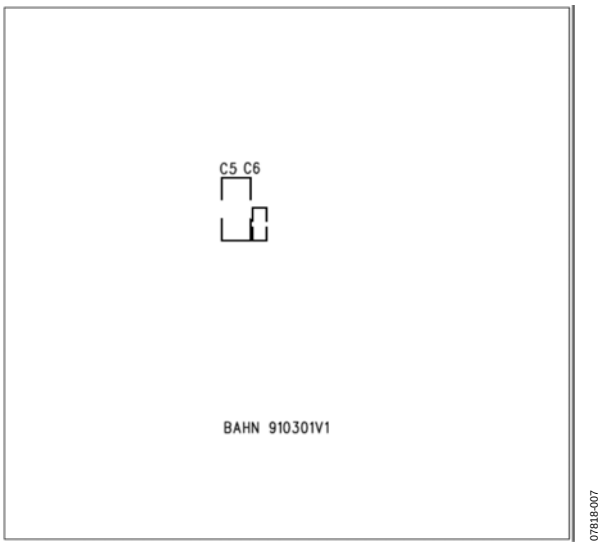

Figure 7. Bottom Silkscreen

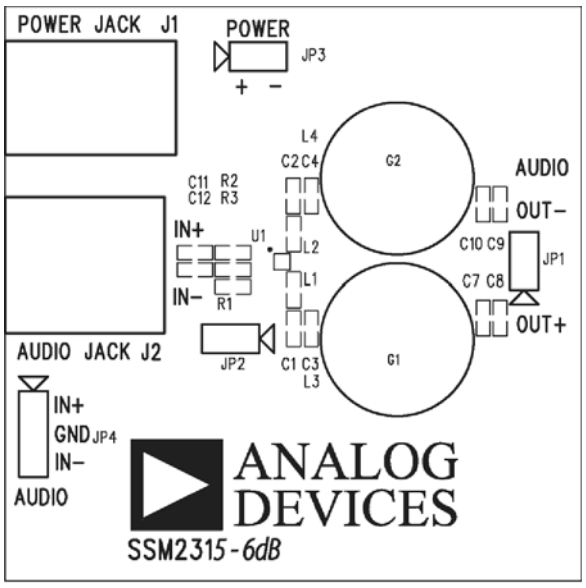

Figure 6. Top Silkscreen

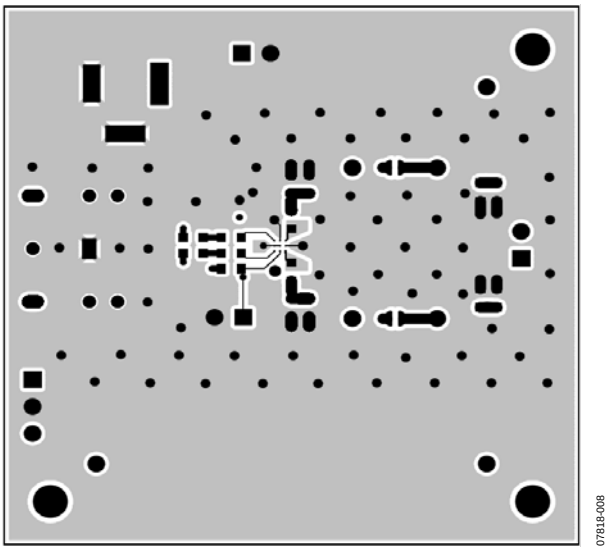

Figure 8. Top Layer

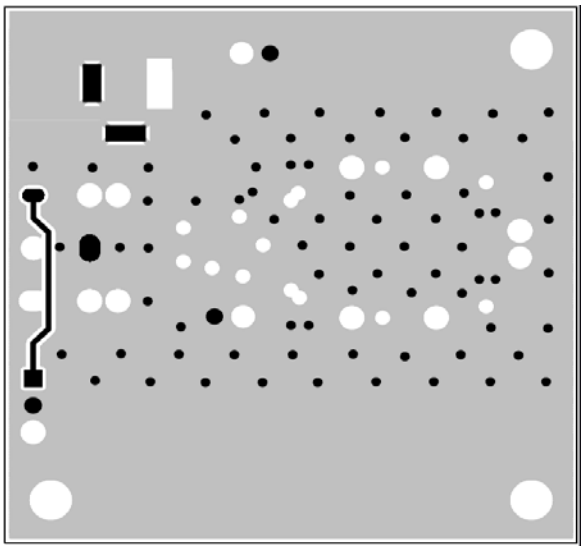

Figure 9. Layer 2 (Ground Plane)

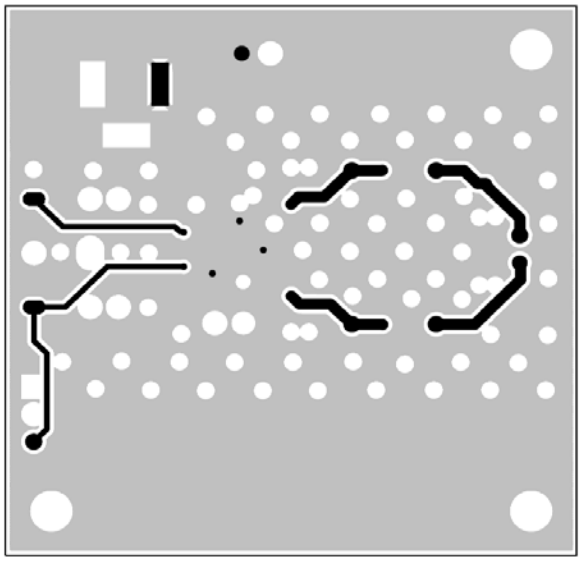

Figure 10. Layer 3 (Power Plane)

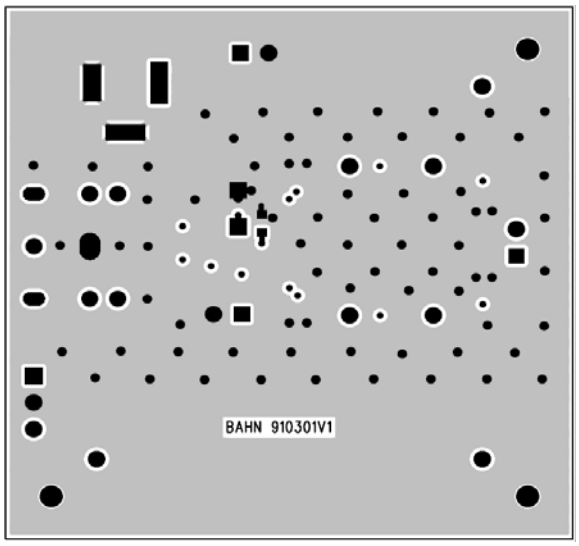

Figure 11. Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

Qty	Reference Designator	Description	Supplier/Part No.
4	C1, C2, C7, C9	Ceramic capacitor, 100 pF, 10%, 50 V, C7 and C9 are not populated	AVX, 06035A101KAT2A
4	C3, C4, C8, C10	Ceramic capacitor, 1 nF, 50 V, C8 and C10 are not populated	Kemet, C0603C102J5GACTU
1	C5	Ceramic capacitor, 10 µF, 10 V	Murata, GRM31MF51A106ZA01L
3	C6, C11, C12	Ceramic capacitor, 0.1 µF, 16 V	Kemet, C0603C104K4RACTU
1	J1	PWRJACK_PJ002A, connector, not populated	CUI, PJ1-021
1	J2	Audio jack, 3.5 mm, 3-pin	CUI, SJ1-3523N
3	JP1, JP2, JP3	HDR1X2, connector header, 2-position	Tyco, 4-103747-0-02
1	JP4	HDR1X3, connector header, 3-position	Tyco, 4-103747-0-03
2	L1, L2	B0603, ferrite chip, 220 Ω, 2 A	TDK, MPZ1608S221A
2	L3, L4	15 µH, not populated	Not populated
1	R1	100 kΩ resistor, 1/10 W, 1%	Yaego, RC0603FR-07100KL
2	R2, R3	0 Ω resistor, 1/10 W, 5%	Yaego, RC0603JR-070RL
1	U1	SSM2315	Analog Devices, SSM2315

ORDERING GUIDE

Model	Description
SSM2315-EVALZ[1]	Evaluation Board

[1] Z = RoHS Compliant Part.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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