# MOSFET

Metal Oxide Semiconductor Field Effect Transistor

# Bare Die

OptiMOS™3 Power MOS Transistor Chip
IPC302N10N3

## Data Sheet

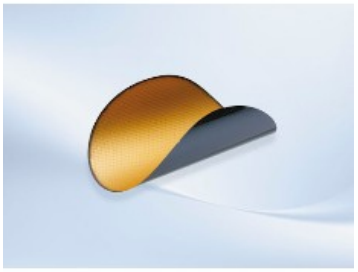
Rev. 2.5
Final

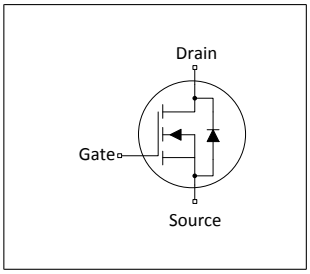
## Industrial & Multimarket

# 1 Description

- N-channel enhancement mode
- For dynamic characterization refer to the datasheet of IPB027N10N3 G
- AQL 0.65 for visual inspection according to failure catalogue
- Electrostatic Discharge Sensitive Device according to MIL-STD 883C
- Die bond: soldered or glued
- Backside metallization: NiV system
- Frontside metallization: AlCu system
- Passivation: nitride (only on edge structure)

Power MOS Transistor Chip






## Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|---|---|---|
| $V_{(BR)DSS}$ | 100 | V |
| $R_{DS(on)}$ | 2.7[1)] | mΩ |
| Die size | 6.7 x 4.5 | $mm^2$ |
| Thickness | 220 | µm |

| Type / Ordering Code | Package | Marking | Related Links |
|---|---|---|---|
| IPC302N10N3 | Chip | not defined | - |

# 2 Electrical Characteristics on Wafer Level

at $T_j$ = 25°C, unless otherwise specified

## Table 2

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 100 | - | - | V | $V_{GS}$=0 V ,$I_D$=1 mA |
| Gate threshold voltage | $V_{GS(th)}$ | 2 | 2.7 | 3.5 | V | $V_{DS}$=$V_{GS}$, $I_D$=302 µA |
| Zero gate voltage drain current | $I_{DSS}$ | - | 0.1 | 1 | µA | $V_{GS}$=0 V ,$V_{DS}$=100 V |
| Gate-source leakage current | $I_{GSS}$ | - | 1 | 100 | nA | $V_{GS}$=20 V ,$V_{DS}$=0 V |
| Drain-source on- resistance | $R_{DS(on)}$ | - | 1.7[2)] | 100[3)] | mΩ | $V_{GS}$=10 V ,$I_D$=2.0 A |
| Reverse diode forward on-voltage | $V_{SD}$ | - | 1.0 | 1.2 | V | $V_{GS}$=0 V ,$I_F$=1A |
| Avalanche energy, single pulse | $E_{AS}$ | - | 45[4)] | - | mJ | $I_D$ =30 A, $R_{GS}$ =25 Ω |

[1)] packaged in a P-TO263-3 (see ref. product)
[2)] typical bare die $R_{DS(on)}$; $V_{GS}$=10 V
[3)] limited by wafer test-equipment
[4)] Wafer tested. For general avalanche capability refer to the datasheet of IPB027N10N3 G

## 3 Package Outlines

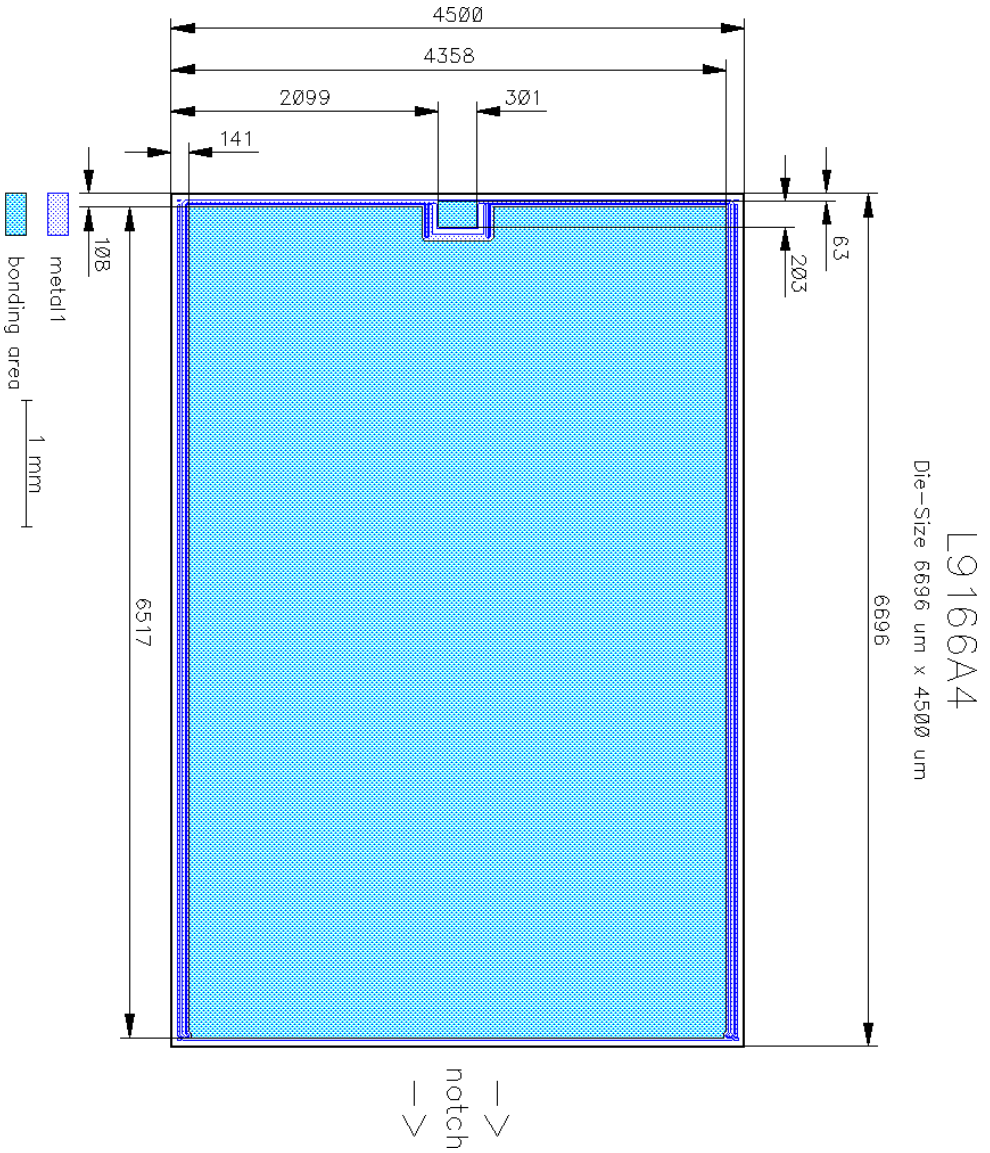



**Figure 1 Outline Chip, dimensions in µm**

## Revision History

IPC302N10N3

**Revision: 2014-07-23, Rev. 2.5**

| Previous Revision | | |
|---|---|---|
| Revision | Date | Subjects (major changes since last revision) |
| 2.5 | 2014-07-23 | Release Final Version |

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